CLAIMS

1. A flash memory device for connecting to a PCI Express-defined bus, the flash memory device comprising:

a flash memory module for storing data;

a connector for connecting to the PCI Express-defined bus, thereby allowing packets to be transmitted between the PCI Express-defined bus and the flash memory device; and

a flash controller for controlling the flash memory module and the connector.

2. The flash memory device of Claim 1, wherein the connector is an ExpressCard connector.

3. The flash memory device of Claim 1, wherein the flash controller includes an analog end unit.

4. The flash memory device of Claim 3, wherein the analog end unit can perform at least one of serial to parallel signal conversion, differential signaling, and phase locking.

5. The flash memory device of Claim 3, wherein the flash controller includes a physical interface engine for extracting transaction layer packet (TLP) information from a signal output by the analog end unit.

6. The flash memory device of Claim 5, wherein the physical interface engine can perform at least one of packet framing/de-framing, 8-bit to 10-bit encoding/decoding, and packet scrambling/de-scrambling.

7. The flash memory device of Claim 5, further including a command register for receiving the extracted TLP.

8. A flash memory device comprising:

flash memory mappable to an address space of a host that is separate from the flash memory device;

a PCI Express-defined connector for allowing the host to communicate with the flash memory device; and

a PCI Express-compatible controller supporting this communication using a command word setting.

9. The flash memory device of Claim 8, wherein the PCI Express-defined connector is an ExpressCard connector.

10. The flash memory device of Claim 8, wherein the PCI Express-compatible controller extracts transaction layer packets (TLPs) from a signal from the host.

11. The flash memory device of Claim 10, wherein each TLP includes at least one of a header, a data payload, and a digest.

12. The flash memory device of Claim 11, wherein the data payload can provide the command word setting, and wherein the PCI Express-compatible controller can respond to the command word setting.

13. The flash memory device of Claim 12, wherein the command word setting includes a command word signature indicating whether the data payload is one of data and the command word setting.

14. The flash memory device of Claim 13, wherein the command word setting includes a data unit transfer length.

15. The flash memory device of Claim 14, wherein the command word setting includes an operation code designating an operation to be performed on the flash memory.

16. The flash memory device of Claim 15, wherein the command word setting includes a logical block address indicating a starting location in the flash memory for the operation.

17. The flash memory device of Claim 16, wherein the command word setting includes a data transfer length based on the data unit transfer length.

18. The flash memory device of Claim 12, wherein the command word setting can indicate an operation to be performed on the flash memory.

19. The flash memory device of Claim 18, wherein the operation can include one of a flash memory read, a flash memory write, a flash memory erase, a direct memory access read, and a direct memory access write.

20. The flash memory device of Claim 12, wherein the command word setting can indicate an operation to be performed on a register of the flash memory device.

21. The flash memory device of Claim 20, wherein the operation can include one of an attribute register read, an attribute register write, and a status register read.

22. The flash memory device of Claim 12, wherein the command word setting can indicate an operation to be performed on the flash memory device.

23. The flash memory device of Claim 22, wherein the operation can include a device reset.

24. A transaction layer packet (TLP) compatible with PCI Express, the TLP comprising:

a header field; and

a data payload field, wherein the data payload field can include a command word setting relating to an operation to be performed on a flash memory.

25. The TLP of Claim 24, wherein the command word setting includes a command word signature indicating whether the data payload includes one of data and the command word setting.

26. The TLP of Claim 25, wherein the command word setting includes a data unit transfer length.

27. The TLP of Claim 26, wherein the command word setting includes an operation code designating an operation to be performed using the flash memory.

28. The TLP of Claim 27, wherein the command word setting includes a logical block address indicating a starting location in the flash memory for the operation.

29. The TLP of Claim 28, wherein the command word setting includes a data transfer length based on the data unit transfer length.

30. The TLP of Claim 24, wherein the command word setting can indicate an operation to be performed on the flash memory.

31. The TLP of Claim 30, wherein the operation can include one of a flash memory read, a flash memory write, a flash memory erase, a direct memory access read, and a direct memory access write.

32. The TLP of Claim 24, wherein the command word setting can indicate an operation to be performed on a register of the flash memory device.

33. The TLP of Claim 24, wherein the command word setting can indicate an operation to be performed on a plurality of registers of the flash memory device.

34. The TLP of Claim 32, wherein the operation can include one of an attribute register read, an attribute register write, and a status register read.

35. The TLP of Claim 24, wherein the command word setting can indicate an operation to be performed using the flash memory device.

36. The TLP of Claim 35, wherein the operation can include a device reset.

37. A method of performing an operation on a flash device, the operation being requested by a host separate from the flash device, the operation being PCI Express-compatible, the method comprising:

sending a first memory request from the host to the flash device, wherein the first memory request includes a header and a command word setting, wherein the command word setting indicates the operation to be performed on the flash device.

38. The method of Claim 37, wherein the header includes a memory mapped I/O address.

39. The method of Claim 38, wherein the memory mapped I/O address includes a command word port.

40. The method of Claim 38, wherein the memory mapped I/O address includes a data value port.

41. The method of Claim 37, wherein if the first memory request is a flash memory write operation, then further including:

sending a second memory request from the host to the flash device, wherein the second memory request includes a header and a data payload, wherein the data payload includes data to be written to the flash device.

42. The method of Claim 41, after receiving the second memory request, further including:

sending a message packet from the flash device to the host, wherein the message packet includes a header and a digest to report on a completion status of the write operation.

43. The method of Claim 37, wherein if the first memory request is a flash memory erase operation, then further including:

sending a second memory request from the host to the flash device, wherein the second memory request includes a header and a dummy data payload, wherein the dummy data payload includes dummy data to be written to the flash device.

44. The method of Claim 43, after receiving the second memory request, further including:

sending a message packet from the flash device to the host, wherein the message packet includes a header and a digest to report on a completion status of the write operation.

45. The method of Claim 37, wherein if the first memory request is a register write operation, then further including:

sending a second memory request from the host to the flash device, wherein the second memory request includes a header and a data payload, wherein the data payload includes data to be written to a register in the flash device.

46. The method of Claim 45, after receiving the second memory request, further including:

sending a message packet from the flash device to the host, wherein the message packet includes a header and a digest to report on a completion status of the write operation.

47. The method of Claim 37, wherein if the first memory request is a memory read operation, then further including:

sending a second memory request from the host to the flash device, wherein the second memory request includes a header and a digest, but no data payload.

48. The method of Claim 47, after receiving the second memory request, further including:

sending a completion packet from the flash device to the host if the read operation is successful, wherein the completion packet includes a header, data from the flash memory, and a digest; and

sending a message packet from the flash device to the host if the read operation is not successful, wherein the message packet includes a header and a digest to report on a completion status of the read operation.

49. The method of Claim 37, wherein if the first memory request is a status register read operation, then further including:

sending a second memory request from the host to the flash device, wherein the second memory request includes a header and a digest, but no data payload.

50. The method of Claim 49, after receiving the second memory request, further including:

sending a completion packet from the flash device to the host, wherein the completion packet includes a header, data from the status register, and a digest.

51. The method of Claim 37, wherein if the first memory request is a direct memory access (DMA) operation, then further including:

sending a second memory request from the flash device to the host.

52. The method of Claim 51, wherein if the DMA operation is a write, then the second memory request specifies a memory-read operation.

53. The method of Claim 52, further including the host:

releasing bus control after receiving the second memory request;

retrieving data requested in the second memory request; and

sending the flash device a completion packet with a data payload.

54. The method of Claim 53, further including the flash device:

issuing a write action; and

allowing data from the host to be written into flash memory.

55. The method of Claim 48, wherein if the DMA operation is a read, then the second memory request specifies a memory-write operation.

56. The method of Claim 55, wherein the second memory request includes a data payload.

57. The method of Claim 56, further including the host releasing bus control after receiving the second memory request.

58. The method of Claim 57, further including the host writing the data payload into system memory according to the second memory request.

59. The method of Claim 58, further including the host sending a message back to the flash device reporting on DMA status.

60. An interface for performing an operation on a memory device, the operation being requested by a Requester separate from the memory device, the interface being PCI Express-compatible, the interface comprising:

sending a first memory request from the Requester to the memory device, wherein the first memory request includes a header and a command word setting, wherein the command word setting indicates the operation to be performed on the memory device.

61. A flash memory controller for controlling a flash memory device, the flash memory controller comprising:

a processor for performing at least one operation; and

arbitration logic coupled to the processor, wherein data from the arbitration logic allows the processor to perform the at least one operation for a flash memory device.

62. The flash memory controller of Claim 61 wherein the flash memory controller can be applied to ExpressCard and also multi-mode USB, Secure Digital (SD), MultiMediaCard (MMC), Memory Stick (MS), and Compact Flash (CF) card .

63. The flash memory controller of claim 61 wherein the flash memory controller provides multiple-block data access.

64. The flash memory controller of claim 61 wherein the flash memory controller provides dual channel processing.

65. The flash memory controller of claim 61 wherein the flash memory controller can perform multiple banks interleave.

66. The flash memory controller of claim 61 wherein the flash memory controller can perform functions of multiple block access, multiple bank interleaving, and multiple channel operations in a memory access cycle.

67. The flash memory controller of claim 61 wherein the flash memory controller can support Single Level Cell (SLC) and Multiple Level Cell (MLC) type of flash memory.

68. A flash memory system including a plurality of flash memory devices, the system comprising:

a first processor;

a device interface coupled to the processor; and

a flash memory controller coupled to the device interface, the flash memory controller comprising:

a second processor for executing at least one operation; and

arbitration logic coupled to the processor, wherein data from the arbitration logic allows the processor to perform the at least one operation for a particular flash memory device of the plurality of flash memory devices.

69. The system of claim 68 wherein the flash memory controller can be applied to ExpressCard and also multi-mode USB, Secure Digital (SD), MultiMediaCard (MMC), Memory Stick (MS), and Compact Flash (CF).

70. The system of claim 68 wherein the flash memory controller provides multiple-block data access.

71. The system of claim 68 wherein the flash memory controller provides dual channel processing.

72. The system of claim 68 wherein the flash memory controller can interleave multiple blocks.

73. The system of claim 68 wherein the flash memory controller can perform functions of multiple block access, multiple bank interleaving, and multiple channel operations in a memory access cycle.

74. The system of claim 68 wherein the flash memory controller can support Single Level Cell (SLC) and Multiple Level Cell (MLC) type of flash memory.

75. A method for managing flash memory in a flash memory system including a plurality of flash memory devices, the method comprising:

(a) initiating at least one operation;

(b) conducting a search for a destination block within a flash memory device; and

(c) relocating valid data within the flash memory device from a source block to the destination block, wherein the at least one operation is performed for a particular flash memory device of the plurality of flash memory devices.

76. The method of claim 75 wherein the method can be applied to ExpressCard and also multi-mode USB, Secure Digital (SD), MultiMediaCard (MMC), Memory Stick (MS), and Compact Flash (CF).

77. The method of claim 75 wherein the flash memory controller provides multiple-block data access.

78. The method of claim 75 wherein the flash memory controller provides dual channel processing.

79. The method of claim 75 wherein the flash memory controller can interleave multiple blocks.

80. The method of claim 75 wherein the flash memory controller can perform functions of multiple block access, multiple bank interleaving, and multiple channel operations in a memory access cycle.

81. The method of claim 75 wherein the flash memory controller can support Single Level Cell (SLC) and Multiple Level Cell (MLC) type of flash memory.

82. A computer readable medium containing program instructions for managing flash memory, the program instructions which when performed by a computer system cause the computer system to perform a method comprising:

(a) initiating at least one operation;

(b) conducting a search for a destination block within a flash memory device; and

(c) relocating valid data within the flash memory device from a source block to the destination block, wherein the at least one operation is performed for a particular flash memory device of the plurality of flash memory devices.

83. The computer readable medium of claim 82 wherein the computer readable medium can be applied to ExpressCard and also multi-mode USB, Secure Digital (SD), MultiMediaCard (MMC), Memory Stick (MS), and Compact Flash (CF) card.

84. The computer readable medium of claim 82 wherein the flash memory controller provides multiple-block data access.

85. The computer readable medium of claim 82 wherein the flash memory controller provides dual channel processing.

86. The computer readable medium of claim 82 wherein the flash memory controller can interleave multiple blocks.

87. The computer readable medium of claim 82 wherein the flash memory controller can perform functions of multiple block access, multiple bank interleaving, and multiple channel operations in a memory access cycle.

88. The computer readable medium of claim 82 wherein the flash memory controller can support Single Level Cell (SLC) and Multiple Level Cell (MLC) type of flash memory.